

EC Project parMERASA: Parallel Execution of Hard Real-Time Programs on Multi-Cores

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- **Demands on Embedded Processors**
- **Predecessor project MERASA** achievements
- **parMERASA project** overview and targets
- **Conclusions and Vision**

- **Increasing demand** for functionality in current and future real-time embedded systems
- Often demand for **mixed application** execution

Increase of processor performance demanded



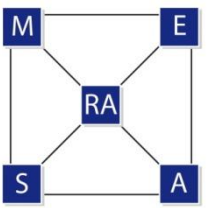
- **Time is critical** in embedded systems!

- Safety-related **hard real-time** embedded systems...
 - require that a **deadline must never be missed**,
 - need a **proof of timing requirements by WCET (worst case execution time) analysis**, or
at least, demonstrate, to an appropriate level of rigour (depending on the criticality of system), that the **implementation meets its timing requirements**.

- **Multi-core processors** provide a solution for **higher levels of performance** of embedded hard real-time systems.
- However, **timing behaviour of parallel applications is not analysable** with current timing analysis techniques.
- **New hardware and software design paradigms** together with **new analysis techniques** are required.

- **COTS (common of-the shelf) processors** contain features that make a WCET analysis hard or even impossible
- **COTS multi-core processors** bring in additional handicaps for hard real-time tasks
- COTS (multi-core) processors are designed for **high average performance, not for timing predictability**

- Our solution based on multi-core systems:
 - Exemplary **parallelisation of industrial applications**,
 - **parallelisation support techniques**,
 - in concert with **WCET technology, verification tools, system architecture**,
 - and **multi-core embedded processor** technology.
- **parMERASA project** (2011-2014) is application-driven and is based on
- **predecessor project MERASA** (2007-2010), which was hardware-driven.



- **Predecessor project: MERASA multi-core architecture**
 - **Timing-predictable** (bus-based) **multi-core** architecture based on **in-order SMT cores**
 - One **hard real-time** task per core in **isolation**
 - Capable of **mixed execution** of hard real-time and non real-time applications
 - System software and tool support (Ottawa and RapiTime)

Hard real-time support by full **isolation of tasks** and **bounding of interferences** can be reached. However, MERASA design not scalable over 4-8 cores.

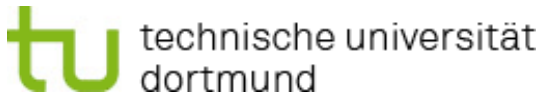
Multi-Core Execution of *parallelised* Hard Real-Time Applications Supporting Analysability

EC FP-7 project started: Oct. 1, 2011, 3 years

3.3 Mio € EC contribution

Project webpage: <http://www.parmerasa.eu>

- Find ways to **efficiently parallelise industrial applications** for embedded real-time systems.
- Provide **hard real-time support in system software, WCET analysis and verification tools for multi-cores.**
- Develop techniques for **time predictable multi-cores with 16 to 64 cores** which are commercially feasible.
- Contribute to **Standards** and **Open Source Software.**



- ▶ **University of Augsburg** (Project Coordinator)
Germany
- ▶ **Barcelona Supercomputing Center**
Spain
- ▶ **Université Paul Sabatier**
Toulouse, France
- ▶ **Technical University of Dortmund**
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- ▶ **Rapita Systems Ltd.**
York, UK
- ▶ **Honeywell international s.r.o.**
Brno, Czech Republic
- ▶ **BAUER Maschinen GmbH**
Schrobenhausen, Germany
- ▶ **DENSO Automotive Deutschland GmbH**
Eching, Germany

- O1: Software engineering approach targeting WCET-aware parallelisation techniques and parallel execution patterns
 - Development path leading from sequential legacy programs to parallel programs
 - **Find at least four patterns that are analysable**
- O2: Parallelisation of industrial case studies by applying the software engineering approach and suitable parallel execution patterns.
 - **Achieve at least an eightfold WCET speedup.**
- O3: On target verification tools
 - **WCET analysis with less than 25% pessimism on WCET estimates of parallel programs.**
 - Tools for code coverage, memory analysis, parallel program profiling and visualisation.
- O4: System architecture and system-level SW that supports WCET analysable parallelisation
 - Common micro-kernel basis and application domain specific run-time environments

- O5: Scalable and timing analysable multi-core processor
 - at least a **16x average speed-up with 64 cores**
 - simulator prototype able to **simulate at least 500,000 instructions per second.**
- O6: Contribute to standards
 - **at least four recommendations to either automotive or avionics standards.**
 - concept for applying the developed parallel execution patterns to AUTOSAR and the IMA standard ARINC 653.
- O7: Contribute to **Open Source software**
 - software developed at the universities, i.e. the static WCET tool OTAWA, the developed system software and the parMERASA simulator, will be made publicly available under an Open Source license at the end of the parMERASA project.

- **Hard real-time demands** in safety critical areas require **timing predictable multi-cores**.
- **MERASA project** showed that **timing predictable multi-core design together with adapted WCET tools and system software** can be achieved
- **parMERASA project** targets **application parallelisation** such that timing predictability can still be guaranteed

- **Application companies** in safety critical areas should **demand timing predictable multi-cores**.
 - WCET analysis and verification instead of or additionally to testing.
- **Safety standards and certifications** should be **tightened to demand such processors**.
- **Higher performance demand** may – in future – be satisfied by **multi-cores with more than 16 cores**.

Make **timing predictable** techniques
commercially feasible to **increase safety** in
aerospace, automation and
automotive domains!